IN THE CLAIMS

Claims 1-30 (Canceled)

31. (New) A semiconductor device, comprising:

a first memory block having a plurality of first memory cells coupled to a plurality of first data lines and a first word line;

a second memory block having a plurality of second memory cells coupled to a plurality of second data lines and a second word line; and

a first block provided between the first and second memory blocks and including a plurality of sense amplifiers,

wherein each of said plurality of sense amplifiers is coupled to one of said plurality of first data lines and one of said plurality of second data lines,

wherein each sense amplifier has a first P type MISFET, a second P type MISFET, a first N type MISFET, and a second N type MISFET,

wherein gates of said first P type MISFET and said first N type MISFET are electrically coupled together, and drains of said second P type MISFET and said second N type MISFET are electrically coupled together,

wherein gates of said second P type MISFET and said second N type MISFET are electrically coupled together, and drains of said first P type MISFET and said first N type MISFET are electrically coupled together, and

wherein a first semiconductor region forming said drain of first P type MISFET is more than half surrounded by a first layer forming said gate of said first P type MISFET.

32. (New) The semiconductor device according to claim 31,

wherein said first layer and a second layer forming said gate of said first N type MISFET are different layers and are connected by a first metal layer formed above said first and second layers.

33. (New) The semiconductor device according to claim 32,

wherein said first semiconductor region is a part of a first active region in a N type well, and

wherein a portion of said first layer surrounding said first semiconductor region is completely formed on top of said first active region.

34. (New) The semiconductor device according to claim 33,

wherein said first and second memory cells are DRAM memory cells,

wherein second and third semiconductor regions each forming said drain and source of said second P type MISFET are a part of said first active region, and

wherein said second semiconductor region forming said drain of said second P type MISFET is more than half surrounded by a third layer forming said gate of said second P type MISFET.

35. (New) The semiconductor device according to claim 34,

wherein said third layer and a fourth layer forming said gate of said second N type MISFET are different layers and are connected by a second metal layer formed above said third and fourth layers, and

said second metal layer is formed in the same metallization level as said first metal layer.

36. (New) The semiconductor device according to claim 35,

wherein a fourth semiconductor region forming said drain of said first N type MISFET is more than half surrounded by said second layer, and

wherein a portion of said second layer surrounding said fourth semiconductor region is completely formed on top of a second active region in a P type substrate.

37. (New) The semiconductor device according to claim 36,

wherein a fifth semiconductor region forming said drain of said second N type MISFET is more than half surrounded by said fourth layer, and

wherein a portion of said fourth layer surrounding said fifth semiconductor region is completely formed on top of said second active region.

38. (New) The semiconductor device according to claim 36,

wherein said first metal layer is connected to said drain of said second P type MISFET through a contact hole and to said drain of said second N type MISFET through a contact hole.

39. (New) The semiconductor device according to claim 38,

wherein said second metal layer is connected to said drain of said first P type MISFET through a contact hole and to said drain of said first N type MISFET through a contact hole.

40. (New) A semiconductor device comprising:

a first memory block having a plurality of first DRAM memory cells coupled to a plurality of first data lines and a first word line;

a second memory block having a plurality of second DRAM memory cells coupled to a plurality of second data lines and a second word line; and

a first block provided between the first and second memory blocks and including a plurality of sense amplifiers,

wherein each of said plurality of sense amplifiers is coupled to one of said plurality of first data lines and one of said plurality of second data lines,

wherein each sense amplifier has a first P type MISFET, a second P type MISFET, a first N type MISFET, and a second N type MISFET,

wherein gates of said first P type MISFET and said first N type MISFET are electrically coupled together, and drains of said second P type MISFET and said second N type MISFET are electrically coupled together,

wherein gates of said second P type MISFET and said second N type MISFET are electrically coupled together, and drains of said first P type MISFET and said first N type MISFET are electrically coupled together,

wherein said gates of said first and second P type MISFETS and of said first and second N type MISFETs are made from separate layers in the same level, respectively,

wherein semiconductor regions each forming said drains of said first and second P type MISFETs are each surrounded on three sides of a rectangle by the gates of said first and second P type MISFETs, respectively, and

wherein semiconductor regions each forming said drains of said first and second N type MISFETs are each surrounded on three sides of a rectangle by the gates of said first and second N type MISFETs, respectively.

41. (New) The semiconductor device according to claim 40, further comprising:

a first metal layer connecting said layer forming said gate of said first P type MISFET and said layer forming said gate of said first N type MISFET, and connecting said drains of said second P type MISFET and said second N type MISFET through contact holes; and

a second metal layer connecting said layer forming said gate of said second P type MISFET and said layer forming said gate of said second N type MISFET, and connecting said drains of said first P type MISFET and said first N type MISFET through contact holes.

42. (New) The semiconductor device according to claim 41,

wherein said plurality of first and second data lines are formed by lithography using phase shift masks.